A MULTIPLE ANTENNA SYSTEM FOR ISM-BAND TRANSMISSION

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ABSTRACT

In this paper we present a multiple antenna system for industrial, scientific, and medical (ISM)-band transmission (MASI). The hardware demonstrator was developed and realized at our institute. It enables multiple input multiple output (MIMO)-communication applications and is capable to transmit arbitrary signals using 8 transmit and 8 receive antennas in parallel. It operates in the 2.4 GHz ISM-band. The hardware concept is introduced and some design specifications are discussed.

Using this transmission system we present some measurement results to show the feasibility of MIMO concepts currently under discussion. The applications include transmit and receive diversity for single carrier and OFDM as well as blind source separation (BSS) techniques.

Keywords: Hardware Demonstrator, MIMO, OFDM, Alamouti, Blind Source Separation

1. INTRODUCTION

One impetus to built a MIMO hardware demonstrator is that the assumptions made about real channels may be incorrect, and the behavior of MIMO systems should be investigated under realistic conditions. Therefore it is sufficient to transmit and receive over a real channel and process the received data offline at the workstation environment. This basic idea roots in [Haa99] where a single antenna system was realized at the University of Bremen. Furthermore, offline processing significantly reduces the complexity of the simulator. In contrast to a realtime simulator, which is based on suboptimal frontend processing (due to strict timing constraints in connection with limited performance of DSP or FPGA chips) [GMea01][BWKD][HWNB03][MLF03], this concept has enabled us to freely investigate optimal and suboptimal algorithm implementations[1]. On the other hand, we do not claim to substitute a MIMO channel sounder [TRT$^+$00]. A channel sounder is a highly accurate measurement system to precisely acquire the (MIMO) channel parameters. This requires extraordinary effort on e.g. calibrated and synchronized time bases at the transmitter and receiver, highly linear frontend amplifiers, and calibrated antenna arrays. In contrast, the objective of our demonstrator is to evaluate MIMO algorithms under non-idealized environments deploying common hardware components. Moreover, thanks to selectable frontend processing we can handle arbitrary radio interface standards, such as single carrier, multicarrier and spread spectrum MIMO systems.

[1]Assuming, that we have an optimal algorithm in idiosyncratic sense, we can neglect implementation issues (quantization errors) on a double-precision machine

2. HARDWARE CONCEPT

2.1. Top-level System Description

The top-level system is diagrammed in Fig. 1. At the workstation environment in-phase and quadrature (I/Q) data, e.g. Hiperlan/2 or UMTS frames, are generated by the simulation system of choice. The impulse shaping is done in the digital domain. The data is scaled and quantized to meet the hardware demonstrator concerns and finally stored into a file. Due to its wide distribution the USB interface is chosen to connect the hardware demonstrator with the workstation. To transfer the I/Q data via the USB interface we use a customized application software which allows us to set several parameters, like sample rate (from external or internal clock), local oscillator (LO) frequency tuning value and assignment of data files to corresponding antennas. Furthermore, in a Matlab environment we can directly access the demonstrator by calling a Matlab function [KK01]. This is useful for fully automated measurements. Inside the demonstrator the I/Q data is stored into digital buffers which are addressed in a circular manner: the increment pointers for memory accesses wrap to the beginning of the buffer when its end is reached. The currently addressed I/Q words are fed to a digital-to-analog converter (DAC), whose analog baseband output signals drive the radio frequency (RF) stage, which performs up-conversion to the desired RF frequency band.

At the receiver, the RF passband signal is down-converted to the complex baseband and undergoes analog-to-digital conversion. A snapshot is stored into a digital buffer.

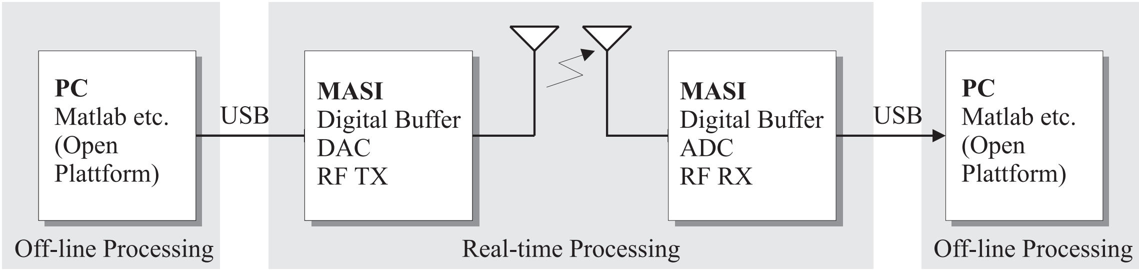

Fig. 1: Principle block diagram

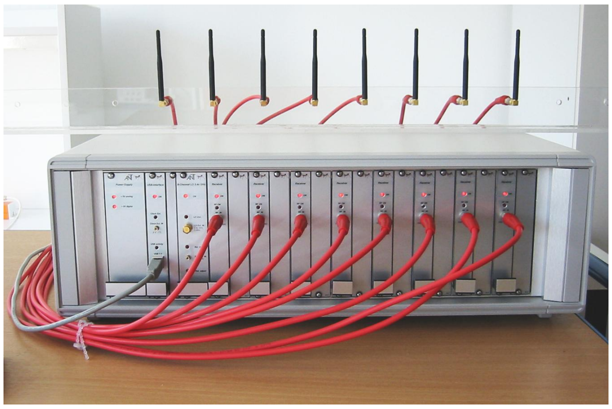

Fig. 2: The Multiple Antenna Receiver for ISM-Band Transmission. Currently, the receiver and transmitter are equipped with 8 modules

Because frame synchronization is not implemented in hardware the receive buffer has doubled length of the transmit buffer to ensure that at least one complete frame is captured. The sample rate is adjustable up to 80 MHz and may be chosen from a set of internally predefined frequencies or an external source. The request for extensibility of the hardware demonstrator led to a full modular architecture; for each antenna the connected transmitter or receiver hardware has its own plug-in module (see Fig. 2). The digital clock and LO signal is provided to all modules by a central clock base to ensure inter module synchronization of sample rate and carrier phase.

Low cost software radios are the main driver for modern radio architectures (universal receivers that can accommodate many different standards). Consequently, this type of receiver gains increased attention. An all digital receiver performs all its operations in the digital domain, except the frontend baseband translation and anti-aliasing filtering. Its ADC sampling clock is not synchronized to the transmitter symbol clock. Therefore, many analog components, such as the voltage-controlled-oscillator (VCO), are not required. Thus, it can be smaller, more robust, and less expensive. However, as a fixed sampling clock is used which is not synchronized to the transmitter clock, symbol timing and carrier recovery have to be accomplished in the digital domain. In order to reduce analog component count in the RF stage the direct conversion (or homodyne) architecture is implemented, which performs passband to baseband translation and vice versa directly without intermediate frequency (IF) stages. Traditionally the direct conversion architecture was considered impractical due to severe realization problems. So far, it was hardly possible to fulfill all requirements like exceptionally linear low noise amplifier (LNA) and mixer circuits, as well as the LO isolation resulting in a lower sensitivity compared to heterodyne receivers [Lee98]. However, recent advances in chip technology enabled robust direct conversion frontends. In the next section we will discuss the employed components and some important parameters in a more detailed manner.

2.2. Detailed Description of Components

The direct conversion architecture leads to very simple RF designs. Extra intermediate frequency (IF) stages with amplifiers, passive bandpass filters and oscillators are omitted, as this simplifies the board design and reduces power dissipation. Furthermore, due to zero IF the image rejection problem does not exist[2]. All subsequent processing can take place at the lowest possible frequency which makes the direct conversion scheme amenable to integrated circuit (IC) implementation. Applying this architecture we are restricted to complex baseband processing which halves the signal bandwidth but doubles the component count in comparison to a passband scheme.

2.2.1. Low Noise Amplifier (LNA)

The first stage of the receiver is a low-noise amplifier (LNA), whose main function is to provide enough gain to overcome

[2] In a heterodyne receiver the first IF is normally chosen relatively high to move the image far away from the desired signal in order to relax the frontend bandpass filter requirements. A direct conversion receiver does not need a frontend filter, however it is practically needed to avoid out-of-band interferes overloading the frontend [Lee98]

the noise of subsequent stages (such as the mixer). Aside from this providing gain while adding as little noise as possible, an LNA should accommodate large signals without distortion. It must also present an impedance of 50Ω to the input source since the transfer function of the preceding filter is quite sensitive to the quality of termination. The employed LNA chip has a gain of 22 dB and a noise figure (NF) of 1.6 dB at 2.4 GHz. A relatively high 1 dB compression point (the input power at which the gain is 1 dB less then expected) of 4.2 dBm and a high third order intercept point (IP3) ensures wide range linear operation.

2.2.2. Mixer

Since for direct conversion architectures the LO frequency lies in the desired frequency band, the LO signal, which normally has much more power than the received signal, can leak into the RF input of the mixer or possibly finds its way to the antenna. The self-mixed LO signal results in a time-invariant DC baseband component, which can drive subsequent stages into saturation. In addition, any even-order distortion produces a DC offset that is signal-dependent, so the second-order intercept point (IP2) is a very important parameter for direct conversion schemes. The employed IC quadrature demodulator has two integrated Gilbert (or four-quadrant) cell mixers. This mixer style provides reasonable conversion gain (IF power output with respect to the RF power input), as well as good rejection at the RF and LO input ports and the IF output due to the complete differential design.

External amplifiers are omitted due to integrated RF and baseband AGC amplifiers, which provide about 70 dB gain control. A high dynamic range is indispensable for wireless application. The baseband I/Q output ports allow direct connection to the ADCs.

2.2.3. Analog-to-Digital Conversion

The analog-to-digital converter (ADC) converts the continuous-time stimuli signals to discrete-time binary-code form. For communications applications the dynamic measures of an ADC, such as signal-to-noise ratio (SNR), spurious-free dynamic range (SFDR) and two-tone intermodulation distortion (IMD) are figures of merit [Wal99]. The effective number of bits (accuracy) depends strongly on these dynamic measurements. High speed ADCs are extremely sensitive to the quality of the sampling clock. The internal track and hold circuit is essentially a mixer. Any noise, distortion, or timing jitter on the clock signal will be combined with the desired signal at the ADC output in addition to internal timing error sources (aperture jitter). A phase-locked loop (PLL) based synthesizer normally exhibits a higher phase noise value than a fixed frequency clock generator. However, to provide several customized sample rates a set of stable crystal-controlled oscillator circuits is used. Furthermore, an external clock input up to 80 MHz is available. The chosen 12bit ADC chip delivers good dynamic measurements, a low aperture jitter and was available at small quantities. The digital outputs (I and Q branches) are directly connected to the digital buffer circuit.

2.2.4. Digital Buffer

The digital buffer stores the raw data, delivered by the ADC (receiver) or provided by the USB-controller (transmitter). At the transmitter the digital buffer serves as a circular buffer. Once the data is completely stored, the buffer is linearly addressed, when the last address is reached the address counter wraps around to the first address and counts up again. Whereas at the receiver only one frame is captured when the trigger event occurs. Because large FIFO chips are very expensive and hardly obtainable at small quantities, the digital buffer circuit is realized by a field programmable gate array (FPGA) and static RAM (SRAM). In contrast to dynamic RAM, SRAM does not need refresh cycles and offers a considerably simpler interface. The employed zero bus turnaround (ZBT) RAMs are fast synchronous SRAM chips which are directly connected to the FPGA. Providing interleaved read/write without wasteful turnaround cycles, the ZBT RAM is predestined for capturing applications. Once primed with an address, it can read/write one word of data per clock cycle. Up to 2^{20} samples can be captured per inphase and quadrature branch. The FPGA connects all digital busses and provides several control signals. Due to the ability of reconfiguration, it offers a high degree of flexibility. It also provides enough resources to hold optional customized frontend processing logic, like frame detection algorithms[3]. The logic blocks are described at a high abstraction level using VHDL[4].

3. MEASUREMENTS AND APPLICATIONS

The measurements were performed in an indoor environment, i.e. we transmitted between two adjacent office rooms of approx. 20 sqm size each. The total transmit power was 17 dBm (50 mW).

3.1. Frame Synchronization

Our system works without any wired connection between the transmitting and receiving end. Therefore we have to

[3]The physical memory (ZBT RAM) has identical size, but the address logic of the circular buffer is programmed according to user settings. Notional, frame synchronization could be implemented in hardware. Thus, the full physical buffer size could be used at transmitter, however, with the drawback of a fixed preamble or frame structure.

[4]Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL)

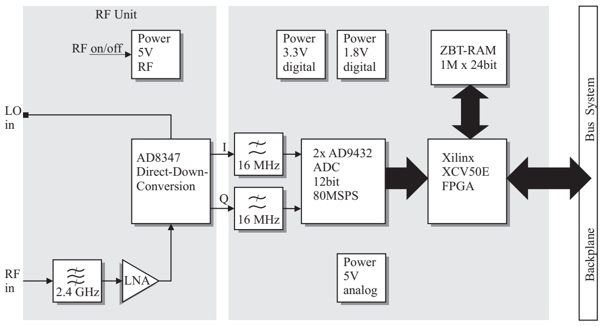

Fig. 3: Receiver module

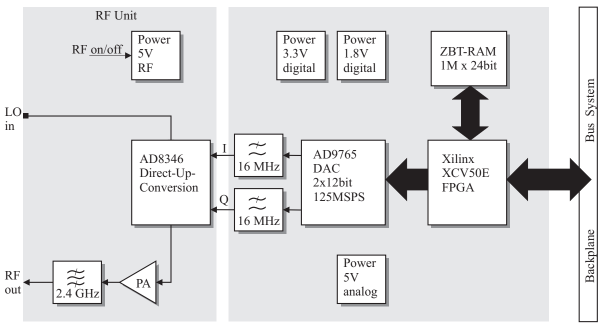

Fig. 4: Transmitter module

synchronize both sides. We transmit periodically repeated frames with L_t samples. In order to get at least one complete frame we sample $L_\mathrm{r} = 2 \cdot L_\mathrm{t}$ values at the receiving side.

The first task is the detection of the starting point of one complete frame within this L_r samples. Therefore we apply a simple power detection scheme, which presents a pragmatic approach for our measurement system, because it is mostly independent from impairments like frequency offset and frequency selective channels, and can be used with any modulation scheme. For the power detection we normally consider about $L_\mathrm{Z} = 1000$ samples within one frame of length L_t. The high variation of the envelope of the signal is unproblematic since we are using a very slow AGC.

Our synchronization approach is a sliding power detection. We detect the current power of the received signal $r(k)$ (one channel) by averaging over L_Z successive samples of both gaps (Fig. 5).

$$
\begin{aligned}
k_\mathrm{start} &= \arg\min_k p\,(k) \\
&= \arg\min_k \sum_{\kappa=k}^{k+L_\mathrm{Z}-1} \frac{1}{2L_\mathrm{Z}} \left(|r\,(\kappa)|^2 + |r\,(\kappa + L_\mathrm{t})|^2 \right) \\
&\quad \text{with} \quad k = 0 \ldots L_\mathrm{t} - L_\mathrm{Z}
\end{aligned} \tag{1}
$$

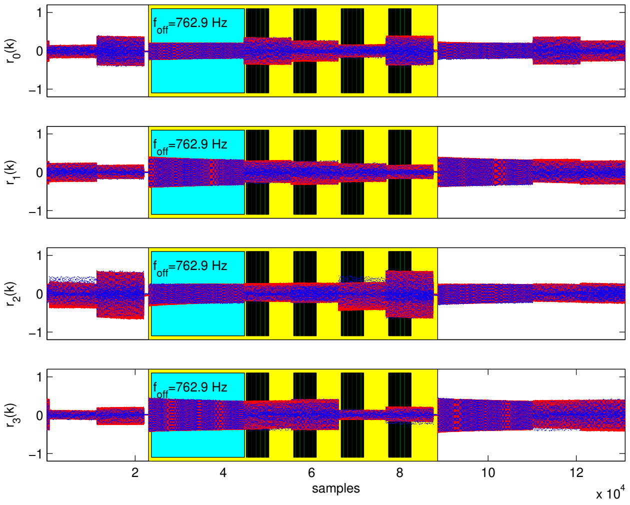

Fig. 5: Measured signals with frame synchronization

This approach for a coarse frame synchronization is not necessarily limited to MIMO setups but can also be used for single input single output (SISO) channels. An example for this scheme is presented in Fig. 5, where you can see time series of a measurement including the detection of the complete frame.

3.2. Frequency Responses

In this section we will present a setup for measuring the frequency response of the MIMO transmission channel, which we always consider from the digital domain at the transmitter to the digital domain at the receiver - including all effects of the system components. We have to emphasize that it is not our intention to do systematic channel measurements.

For measurements we apply a chirp-like signal, whereas only one transmitter is sending at a time, in order to measure the complete matrix of frequency responses (Fig. 6).

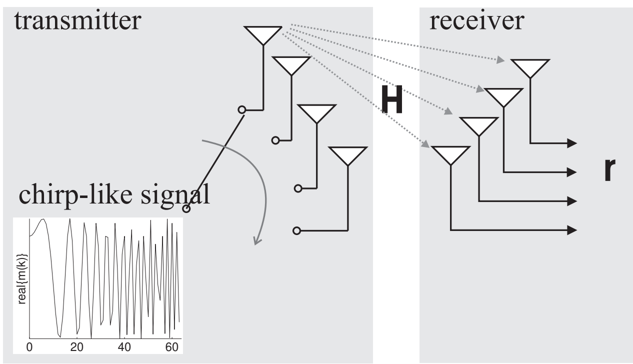

Fig. 6: Multiplexing for channel measurement

This signal is designed in the frequency domain as

$$M(n) = e^{-j\frac{\pi}{N_{\mathrm{DFT}}}n^2} \quad \text{for} \quad n = 0 \ldots N_{\mathrm{DFT}} - 1 \quad , \qquad (2)$$

because this guarantees an exactly flat magnitude. Processing the IDFT, we get the time domain signal

$$m(k) = \mathrm{IDFT}_{N_{\mathrm{DFT}}}\{M(n)\} \qquad (3)$$

which is inherently periodic. We exploit this property and send $m(k)$ in a periodic way so that only a coarse synchronization is necessary.

The quadratic phase increment leads to a small crest factor[5]of the signal. In our case with $N_{\mathrm{FFT}} = 128$ the crest factor for the imaginary part of the signal $m(k)$ is

$$c_{\mathrm{imag}} = \frac{\max \mathrm{imag}\{m(k)\}}{\sqrt{\frac{1}{N_{\mathrm{DFT}}}\sum_{k=0}^{N_{\mathrm{DFT}}-1}\mathrm{imag}\{m(k)\}^2}} \approx 1.47 \quad . \qquad (4)$$

We can measure the frequency response, up to a linear phase uncertainty, by using a fractional part of the received time signal with N_{DFT} samples and calculating

$$\begin{aligned} R(n) &= \mathrm{DFT}_{N_{\mathrm{DFT}}}\{r(k_{\mathrm{offset}} + k)\} \\ & \quad k = 0 \ldots N_{\mathrm{DFT}} - 1 \end{aligned} \qquad (5)$$

$$H(n) = \frac{R(n)}{M(n)} \quad . \qquad (6)$$

Fig. 5 shows the time series of one measurement. Notice the different amplitudes of the signal that correspond to one constellation of the multiplexing scheme (Fig. 6). Since this method is sensitive regarding the frequency offset, we added a pilot sequence to our measurement frame in order to estimate and correct the offset.

The advantage of this approach is that we only need a coarse synchronization and not a high-precision time reference (like in channel sounding setups). Therefore the starting position k_{offset} may be slightly inaccurate. This circular[6] time shift of the starting position will result in a linear phase term, but it does not influence the shape of the magnitude response:

$$\begin{aligned} H_{\mathrm{shift}}(n) &= \frac{\mathrm{DFT}_{N_{\mathrm{DFT}}}\{r(k+k_{\mathrm{shift}})\}}{M(n)} \\ &= H(n)e^{j\frac{2\pi}{N_{\mathrm{DFT}}}nk_{\mathrm{shift}}}. \end{aligned} \qquad (7)$$

Fig. 7 depicts 3 different frequency response measurements using 4 transmit and 4 receive antennas. Uniform linear arrays (ULAs) with $\lambda/2$ spaced elements are used. The sampling frequency was set to $f_s = 50$ MHz.
One directly can see the filter influence of our transmissions system, which limit the signal to the 3 dB range of

[5]The peak-to-rms voltage ratio of an alternating current (AC) signal

[6]Since we are using a periodic repeated signal, we can interpret a time shift as a periodic time shift.

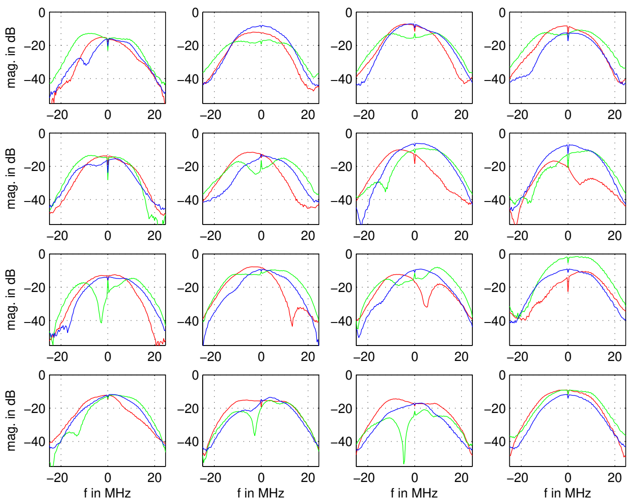

Fig. 7: Frequency responses for a 4x4 setup

approx. ± 16 MHz. In addition there are some notches in the spectrum that arise from a frequency selective channel. Our measurements revealed, that already a small change of the position may have a strong impact on the frequency response.

3.3. Diversity techniques

There are two principle approaches to get a performance gain from an antenna array. One approach uses the known geometric constellation of the antennas for beamforming. The other approach is independent of the array constellation and increases the diversity of the system.

In this section we focus on diversity techniques. Diversity through a multi antenna setup can be attained at the receiving as well as at the transmitting end.

3.3.1. Receive diversity

In order to achieve a diversity gain at the receiving side we can expand a SISO setup and use multiple receive antennas. The diversity combining can be done in a blind way by using the spatial covariance of the received signal streams. Timing offset is estimated after combining using the approach presented in [Lee02].

For combining we have to take into account that our system has independent AGCs in each channel. Therefore we have to estimate the noise level, which is done by exploiting the power gap in the frame of the received signal.

In order to show the gain of a combining we sent one QPSK signal and received it with multiple antennas. Fig. 8 depicts the signal constellations of a measurement. On the left hand side you can see the signal constellations received from each antenna, while the right hand side depicts the

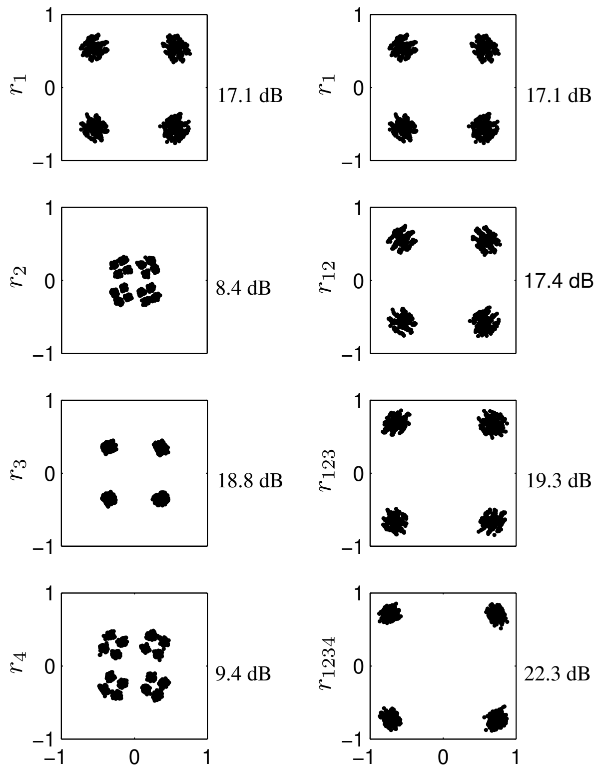

Fig. 8: Combining gain with estimated SNR

combining of the signals received by antenna one up to four. The rising SNRs for increasing number of signals involved in the combining process indicate the combining gain.

SNR estimation is done using the approach presented in [Mat93], because it doesn't suffer from wrong symbol decisions and is suitable without modification for all PSK schemes. The SNR of a single data stream y is calculated by

$$p = \sqrt{2 - \frac{\mathrm{E}\left\{|y|^4\right\}}{\mathrm{E}\left\{|y|^2\right\}^2}} \tag{8}$$

$$SNR = \frac{p}{1-p} \quad . \tag{9}$$

3.3.2. Transmit Diversity

In theory, receive diversity and transmit diversity are interchangeable. In the following we will discuss transmit diversity schemes, especially the so called orthogonal space-time block codes (OSTBC), under more realistic conditions. Channel estimation and carrier offset estimation are essential tasks in coherent receivers. However, they are also some kind of error sources due to the imperfectness of the employed algorithm.

Alamouti [Ala98] discovered a remarkable transmit diversity scheme for transmission with two antennas. This scheme supports maximum-likelihood detection based only on linear processing at the receiver and is able to achieve full diversity provided by the number of transmit and receive antennas. The input symbols to the ST block encoder are divided into groups of two symbols each $\{s_1, s_2\}$. At a given symbol period, s_1 and $-s_2^*$ are transmitted from antenna 1 and 2, respectively, and at the consecutive symbol period, s_2 and s_1^* are transmitted from antenna 1 and 2, respectively. Let h_1 and h_2 be the channel coefficients from the first and second transmit antennas, respectively. It is assumed that h_1 and h_2 are constant over two consecutive symbol periods. Consider a receiver with one receiver antenna and denote the received signals over two consecutive symbol periods as r_1 and r_2. Defining the code symbol vector $\mathbf{s} = [s_1 s_2^*]^T$ and the received vector $\mathbf{r} = [r_1 r_2^*]^T$, we get

$$\mathbf{r} = \mathbf{H}\mathbf{s} + \boldsymbol{\eta} \tag{10}$$

where the channel matrix

$$\mathbf{H} = \begin{bmatrix} h_1 & -h_2 \\ h_2^* & h_1^* \end{bmatrix}, \tag{11}$$

and the noise vector $\boldsymbol{\eta} = [\eta_1 \eta_2]^T$ are used. The AWGN is represented by η_1 and η_2 which are modelled as i.i.d complex Gaussian random variables with zero mean and power spectral density $N_0/2$ per dimension. Hence $\boldsymbol{\eta}$ is a Gaussian random vector with zero mean and covariance $N_0\mathbf{I}$.

The decoding procedure consists of a simple multiplication with the hermitian channel matrix $\hat{\mathbf{H}}^H$, hence

$$\tilde{\mathbf{r}} = \hat{\mathbf{H}}^H \mathbf{H}\mathbf{s} + \hat{\mathbf{H}}^H \boldsymbol{\eta} \tag{12}$$

where $\hat{\mathbf{H}}$ is the *estimated* channel matrix. Considering imperfect channel estimation with an estimation error [SBF01]

$$\Delta h = \Delta h_{\text{noise}} + \Delta h_{\text{Doppler}} \tag{13}$$

it follows

$$\hat{\mathbf{H}} = \begin{bmatrix} h_1 + \Delta h_1 & -(h_2 + \Delta h_2) \\ h_2^* + \Delta h_2^* & h_1^* + \Delta h_1^* \end{bmatrix}. \tag{14}$$

The (soft) decoded symbol-vector $\tilde{\mathbf{r}} = [\tilde{r}_1 \tilde{r}_2^*]^T$ can be obtained using (12) and (14)

$$\tilde{\mathbf{r}} = \underbrace{\begin{bmatrix} |h_1|^2 + |h_2|^2 & 0 \\ 0 & |h_1|^2 + |h_2|^2 \end{bmatrix} \mathbf{s}}_{\text{desired}} \tag{15}$$

$$+ \underbrace{\begin{bmatrix} h_1 \Delta h_1^* + h_2^* \Delta h_2 & -h_2 \Delta h_1^* + h_1^* \Delta h_2 \\ -h_1 \Delta h_2^* + h_2^* \Delta h_1 & h_2 \Delta h_2^* + h_1^* \Delta h_1 \end{bmatrix} \mathbf{s}}_{\text{influence of estimation errors}}$$

$$+ \underbrace{\hat{\mathbf{H}}^H \boldsymbol{\eta}}_{\text{noise}}$$

From (15) it is clear that channel estimation errors lead to spatial intersymbol interference (ISI) if the estimated channel matrix $\hat{\mathbf{H}}$ is not unitary. (14).

Another major task for coherent receivers is the carrier frequency offset estimation and correction. Consider two consecutive received symbols r_1 and r_2. The frequency offset can be modelled by the time-domain multiplication with the two phasors $e^{j\varphi_1}$ and $e^{j\varphi_2}$, respectively. Using the system model (10) it can be stated

$$\begin{bmatrix} e^{j\varphi_1} & 0 \\ 0 & e^{-j\varphi_2} \end{bmatrix} \begin{bmatrix} r_1 \\ r_2^* \end{bmatrix} = \begin{bmatrix} e^{j\varphi_1} & 0 \\ 0 & e^{-j\varphi_2} \end{bmatrix} (\mathbf{Hs} + \boldsymbol{\eta}). \quad (16)$$

Assuming perfect channel estimation conditions, i. e. $\hat{\mathbf{H}} = \mathbf{H}$, and neglecting the noise term in (16), we obtain

$$\begin{bmatrix} h_1^* & h_2 \\ -h_2^* & h_1 \end{bmatrix} \begin{bmatrix} e^{j\varphi_1} & 0 \\ 0 & e^{-j\varphi_2} \end{bmatrix} \begin{bmatrix} h_1 & -h_2 \\ h_2^* & h_1^* \end{bmatrix} \mathbf{s}$$

$$= \begin{bmatrix} |h_1|^2 e^{j\varphi_1} + |h_2|^2 e^{-j\varphi_2} & -h_1^* h_2 e^{j\varphi_1} + h_2 h_1^* e^{-j\varphi_2} \\ -h_2^* h_1 e^{j\varphi_1} + h_1 h_2^* e^{-j\varphi_2} & |h_2|^2 e^{j\varphi_1} + |h_1|^2 e^{-j\varphi_2} \end{bmatrix} \mathbf{s}. \quad (17)$$

In contrast to a single transmit antenna system, the loss of orthogonality due to a (residual) frequency offset leads to *magnitude* variations. A comparison of a simulated and a measured signal constellation with channel estimation and frequency offset is depicted by Fig. 9.

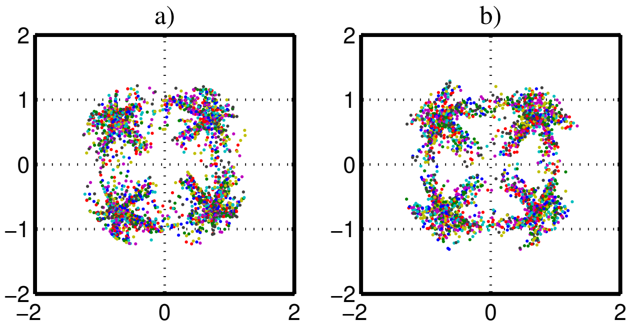

Fig. 9: QPSK signal constellations at the STBC decoder output: a) simulated signal, b) measured signal

3.4. OFDM Transmission

Our simulation tool for OFDM transmission is based on the IEEE 802.11a WLAN standard [IEE99], except for the carrier frequency of 2.4 GHz (instead of 5.2 GHz).

3.4.1. Synchronization

Timing Synchronization - First of all, a coarse frame synchronization according to the method for single carrier systems already described (3.1) is carried out. For OFDM transmission, there is no need finding the starting point of the burst exactly, because afterwards the position of the FFT window is adjusted in a second synchronization step.

Due to the cyclic prefix in every OFDM symbol, the exact position of the FFT window can be found by correlation over the received signal. This results in a well defined maximum value for each OFDM symbol, the correct FFT window start position is N_{guard} samples later. Averaging OFDM symbols to suppress noise may be reasonable.

Carrier Frequency Synchronization - The correction of carrier frequency offsets (CFO) in OFDM systems can be carried out in two steps. A synchronization in time domain (before processing the FFT at the receiver) is absolutely necessary, because severe intersymbol interference (ISI) occurs in frequency domain if a CFO is not corrected before. In case of small frequency offsets (compared with the subcarrier spacing) the main effect after processing the FFT is a rotation of symbols regarding their signal constellation, so that in time domain a coarse synchronization is sufficient. This coarse estimation is accomplished by calculating the phase deviation between the two preamble C symbols [IEE99].

A fine carrier frequency synchronization in frequency domain is based on the 4 pilot symbols which are included in every OFDM symbol and whose carrier positions are symmetric to the carrier with frequency $f = 0$. The pilot carriers are BPSK modulated. To estimate the CFO from the pilot symbols, the channel coefficients according to these carriers have to be known. Because every OFDM symbol carries the pilot information, a tracking of the CFO estimation can easily be performed. For further details on our synchronization methods see [Sch01].

3.4.2. Impact of a DC Offset

A DC offset, e.g. resulting from self mixing of the oscillators as described in 2.2, is a serious problem when using direct conversion concepts. With regard to a transmission, we have to take into account different aspects. On the one hand, the coarse burst synchronization fails with signals having high DC offsets. Therefore, it is necessary to average the whole received sequence to get an estimate for the DC offset and to subtract it afterwards. On the other hand, assuming a correct synchronization, the impact of the DC offset at the receiver in frequency domain is, due to the rectangular windowing of the FFT, the same as an addition of a sinc function with the maximum at $f = 0$ and zero crossing at all other subcarrier frequencies. That is why the DC subcarrier is unassigned in IEEE 802.11a. In fact, this is no solution, because in combination with a carrier frequency offset the DC offset affects *all* subcarriers. In this case, the sinc function's maximum is shifted by the value of the CFO and additionally the zero crossings move *between* the sampling points of the subcarriers.

Fig. 10 (left hand side) shows the signal constellation diagram of a 54 Mbit/s data burst transmitted with our system at 2.4 GHz after equalization. The received signal contains a DC offset of approx. 7 dB (ratio of DC magnitude to rms[7] of signal without DC) and a CFO of approx. 104 kHz.

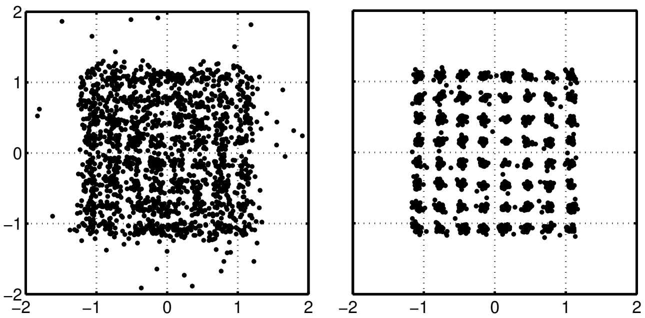

Fig. 10: Impact of a DC offset (7 dB): signal constellation diagram (uncorrected/corrected)

When correcting the DC offset, an estimation based on averaging a certain number of preamble B symbols in time leads to sufficient results (see Fig. 10, right hand side).

3.4.3. Transmit Diversity Schemes for OFDM

Considering transmit diversity schemes for IEEE 802.11a, one can distinguish between schemes which are compatible to the standard and those which are not. Space time block codes (STBC) belong to the latter ones. In contrast, delay diversity schemes need no modification of the receiver at all, thus they are fully standard conform.

Delay Diversity and Cyclic Delay Diversity - Delay diversity means transmitting the same OFDM symbol in time domain, including the cyclic prefix, with a certain delay for each antenna. Due to synchronization constraints, the maximum delay is restricted to the remaining length of the cyclic prefix, which is the total length of the cyclic prefix minus the channel impulse response length. A better solution especially for OFDM systems is *cyclic* delay diversity (CDD), e. g. known from [DK02] and [BC02]. Using cyclic delay diversity, cyclically time-shifted OFDM symbols are *simultaneously* transmitted by each antenna. It is important to note, that the signal is shifted *before* inserting the cyclic prefix (CP). Compared to noncyclic delay diversity there is no strong restriction for the length of the delay. The allowed maximum length equals to the FFT length.

The principle of all delay diversity schemes is to increase the length of the channel impulse response seen at the receiver, i. e. the channel transfer function becomes more frequency selective. The added diversity is only exploited by the channel decoder [BC02], in contrast to other transmit diversity schemes there is no SNR enhancement. Because the superposition of the transmitted signals from each antenna at the receiver using delay diversity or cyclic delay diversity is equivalent to a single transmit antenna system with extended channel impulse length, no changes are necessary at the receiver.

Fig. 11 shows the increased frequency selectivity due to CDD by means of two measured channel transfer functions at 2.4 GHz. To the right, a CDD system with 2 transmit antennas and a delay of 6 samples ($\equiv 0.3\mu$s) was used. For comparison the single antenna case is presented in the left figure. The magnitudes of the channel coefficients for each subcarrier in the OFDM system were obtained by the estimation based on the IEEE 802.11a preamble.

Although there is no restriction for the delay length using CDD in theory, problems may occur if a noise reduction (NR) of the estimated channel transfer function by windowing in time domain [Sch01] is carried out. In this case, the *increased* channel impulse length due to CDD has to be considered when fixing the NR window length. If the window length is too short, the channel impulse response will be falsified which significantly reduces the performance of the NR.

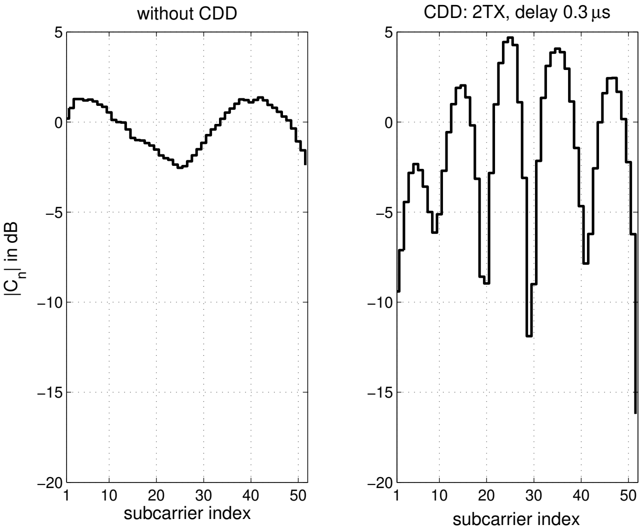

Fig. 11: Measured channel transfer functions

STBC: Alamouti Scheme - The transmit diversity scheme proposed by Alamouti [Ala98] is based on non frequency selective or flat fading channel assumptions. Therefore, in case of OFDM the coding of the transmit symbols according to Alamouti has to be done in *frequency* domain, i.e. before processing the IFFT at the transmitter, and decoding after applying the FFT at the receiver. So in contrast to delay diversity schemes, two IFFT processing units are needed. Because the OFDM demodulation (FFT) is the inverse oper-

[7] root mean square: $\sqrt{1/N \sum_{k=1}^{N} |s(k)|^2}$

ation of the modulation (IFFT), the equations describing the Alamouti coding (10) remain unchanged for OFDM transmission, except for the transmit symbols s_i as well as the receive symbols r_i becoming OFDM symbols in frequency domain, i.e. they consist of 52 (number of subcarriers) PSK or QAM symbols each.

In contrast to all delay diversity schemes, using the Alamouti transmit diversity scheme is *not* compatible to IEEE 802.11a. In addition to the modifications in the receiver according to the Alamouti decoding, a modification of the channel estimation and synchronization algorithms as well as a new preamble structure is necessary.

3.4.4. Receive Diversity Scheme for OFDM

The application of receive diversity to a transmission system based on IEEE 802.11a can be realized without any changes to the transmitter, i.e. absolutely standard conform. One possible method is maximum ratio combining (MRC), on which we will focus in the following.

Maximum Ratio Combining - In order to combine the received symbols according to the MRC principle, in frequency domain, the not yet equalized values on each subcarrier are multiplied with the corresponding conjugate complex channel coefficient. The resulting values of all receive antennas are then added up separately for each subcarrier and afterwards, in case of QAM symbols, normalized to the sum of power of the channel coefficients resulting from the different antennas. After a soft-decision demapping, the weighted bits are multiplied with the inverse of the normalization factors used before.

A measurement example obtained with MASI can be seen in Fig. 12. In that case, the BER for the signal received on the first and second receive antenna after channel decoding is 0.11 and 0.5, respectively. MRC of the two received signals (s. Fig. 12c) results in a reduction of the BER to $7.97 \cdot 10^{-3}$, whereas the combining of four receive signals (s. Fig. 12d), obtained with two additional receive antennas, leads to an error-free reception.

3.5. Blind Source Separation

Blind source separation (BSS) algorithms are able to separate different signals from a multi sensor setup. The only knowledge used to achieve this goal is that the signals should be statistically independent.

To apply source separation techniques in communications we are using the setup depicted in Fig. 13. First of all the DC-offset caused by the direct conversion frontend is removed. After root raised cosine filtering a frame synchronization according to section 3.1 is carried out. To separate the independent components we can apply a BSS algorithm directly to the oversampled signal. For this step we choose

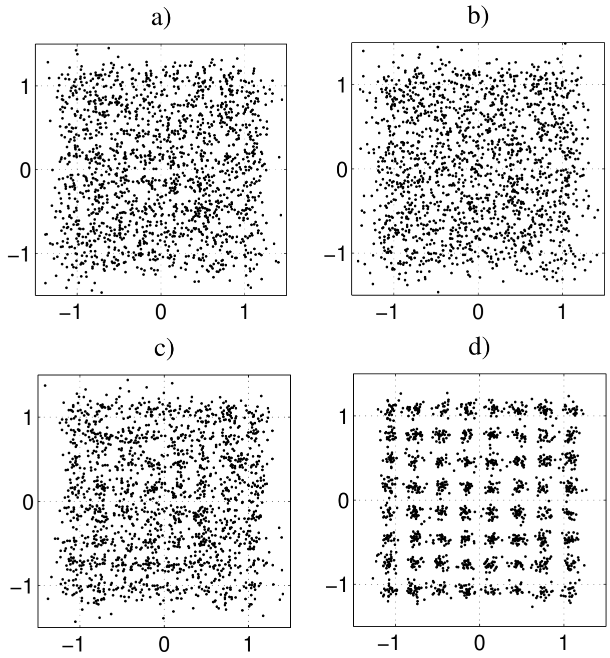

Fig. 12: Signal constellations: a) receive signal 1, b) receive signal 2, c) MRC of receive signals 1 and 2, d) MRC of receive signals 1 to 4

the JADE [CS93] algorithm[8] as a spatial only separation approach.

The separation leads to data streams which are processed in the classical way like in single antenna systems. We synchronize to the symbol timing using the method presented in [Lee02]. In order to determine the carrier frequency offset we apply a non-linearity and a frequency estimation.

Measurements were done with a sampling frequency of $f_s = 10$ MHz in order to get an approximately flat channel.

[8]We also successfully used other approaches like fastICA [BH00] and SSARS [FK98].

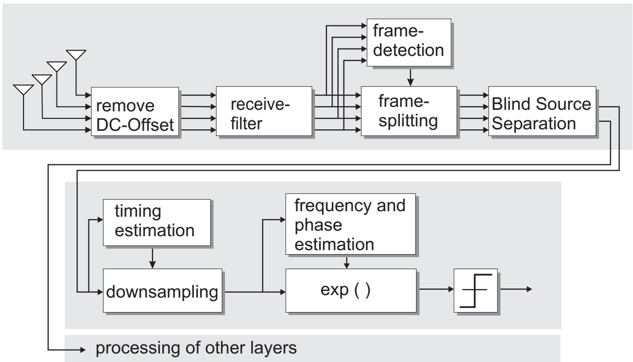

Fig. 13: BSS setup

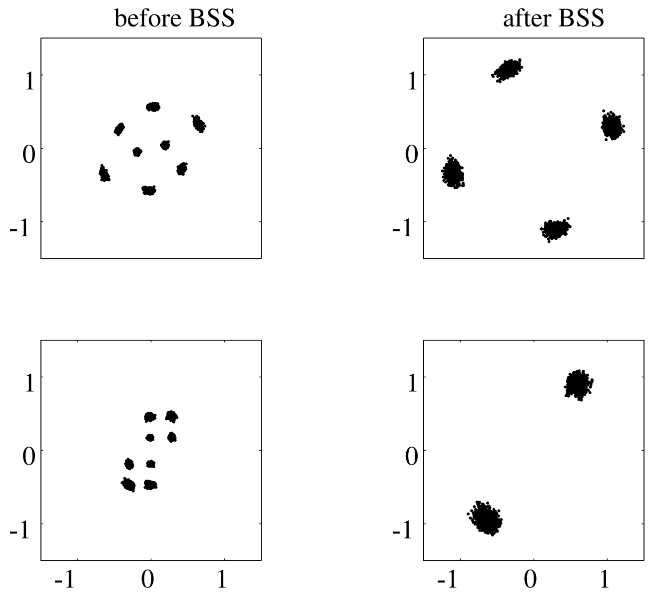

Fig. 14: 2x2 signal constellations before and after BSS

In order to visualize the successful separation we simultaneously transmit signals with different modulation schemes.

Fig. 14 depicts the separation of a BPSK and a QPSK signal sent in parallel and received by two antennas. The signal constellation before separation is obtained by using the timing information estimated after separation. As one can see in Fig. 14 the signal streams are properly separated. The graphs on the left show that in this particular measurement the signal of the BPSK signal was dominant.

The separation procedure can be easily extended to a system with four transmit and receive antennas. The results are depicted in Fig. 15. It can be seen that even in this situation a proper blind separation is possible.

Based on our experiences we can state that it is practically possible to apply separation algorithms for separation of communication signals in MIMO setups, even if the properties of the modulation schemes are not taken into account. This makes our setup interesting for interference scenarios. If a knowledge of the symbol alphabet of a signal is additionally exploited, the BSS can be used as a frontend to spatial interference cancellation algorithms like VBLAST [WFGV98].

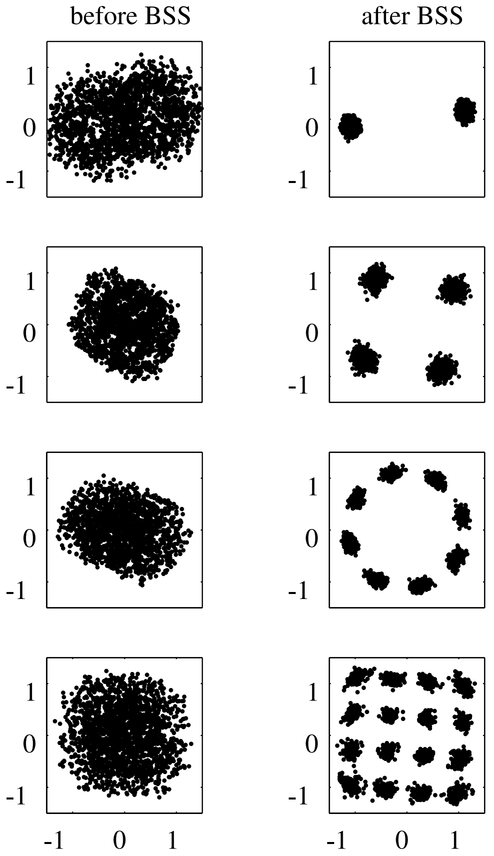

Fig. 15: 4x4 signal constellations before and after BSS

4. CONCLUSIONS

In this paper we introduced a very flexible low cost measurement system which allows the testing of nearly all MIMO communications setups currently under discussion. Arbitrary signals can be generated and transmitted in real time. However, the offline processing concept significantly reduces the complexity of the demonstrator. In contrast to a realtime simulator, this has enabled us to freely investigate optimal and suboptimal algorithms. Moreover, we are not limited to a special simulation software. A wide range of applications was presented. In order to show the nature of the MIMO channel we accomplished some indoor measurements of frequency responses. Furthermore, receive and transmit diversity schemes to gain performance from the spatial channel were considered. In theory, receive and transmit diversity are interchangeable. However, in practice we observed that orthogonal STBCs are more sensitive to estimation errors. As an example for OFDM, we evaluated a system according to IEEE 802.11a to which we successfully applied several transmit and receive diversity schemes. The feasibility of BSS for communications systems under realistic conditions was studied. During our indoor measurements we could hardly produce scenarios that prevent the BSS from working. Consequently, BSS algorithms, which can be directly applied to the oversampled received signal without timing and carrier offset synchronization, are suitable for robust frontend processing.

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